Analog CMOS Computing Chips for Fast and Energy-Efficient Solution of PDE Systems

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3/15/2022

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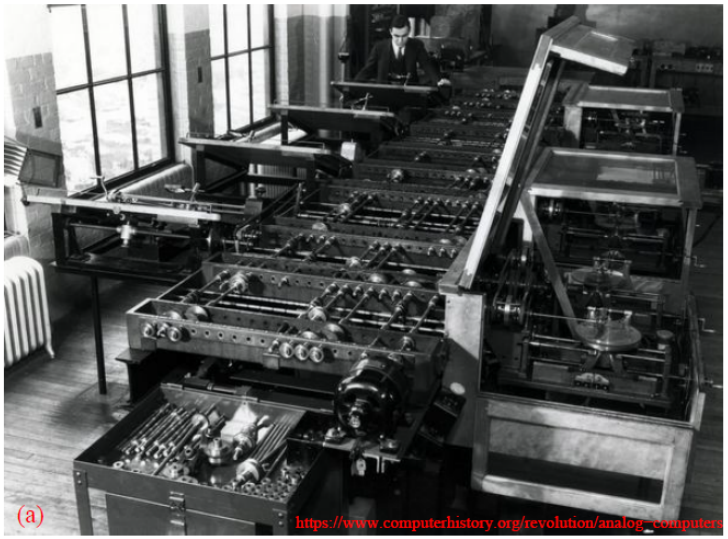
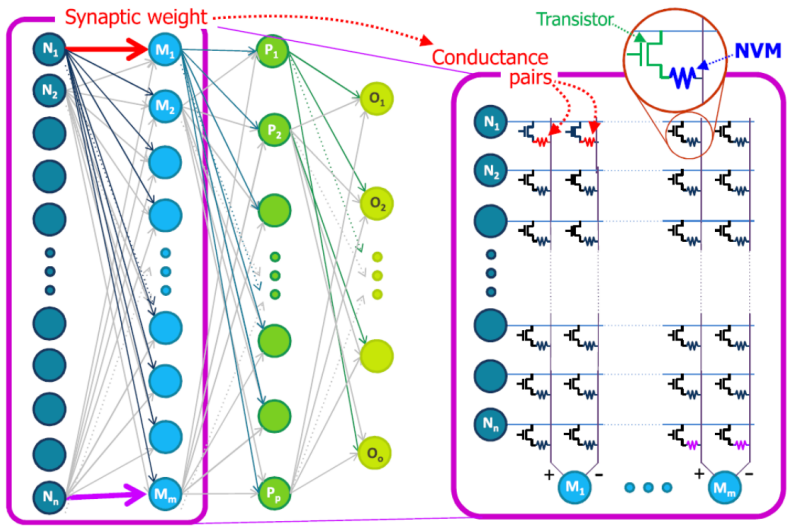
Outline

Analog Computing

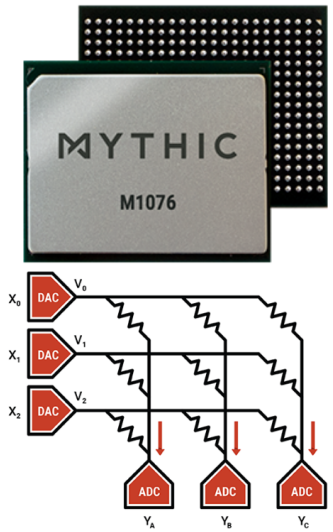


- Analog computers (ACs) were the primary method of computation in 1930s - 1940s [1]. In 1948, the Reeves instrument corporation (RICO) became the first company to market a complete general-purpose analog computer [2, 3].
- The invention of digital computers followed by transistor scaling surpassed analog computing over the last few decades [1, 4].
- However, digital computing hardware and algorithms are no longer improving exponentially as Moore's law slows down [5]. This has led to the exploration of alternative technologies.

Analog Computer for Machine Learning



Source: P. Narayanan *et al.*, "Toward on-chip acceleration of the backpropagation algorithm using nonvolatile memory," in *IBM Journal of Research and Development*, vol. 61, no. 4/5, pp. 11:1-11:11, 1 July-Sept. 2017



https://www.mythic-ai.com/product/m1076-analog-matrix-processor/

- Analog circuits can exploit the physics of transistors in implementing computational primitives for DNNs [6–8].
- Analog computing allows the implementation of efficient vector-matrix multiplications (VMMs).
- Weight values of the matrix can be stored as conductance values of the crossbar array.
- In-memory computing finds applications in machine learning.

State of the Art Analog Computers

BrainScaleS-1

https://ebrains.eu/service/neuromorphic-computing/#BrainScaleS

The Analog Thing

https://the-analog-thing.org/

N. Guo, Y. Huang, T. Mai, S. Patil, C. Cao, M. Seok, S. Sethumadhavan, and Y. Tsividis, "Energy-Efficient Hybrid Analog/Digital Approximate Computation in Continuous Time", IEEE Journal of Solid-State Circuits, July 2016.

https://www.mythic-ai.com/product/m1076-analog-matrix-processor/

Analog Computer for Solving Partial Differential Equations (PDEs)

Analog Computing Research

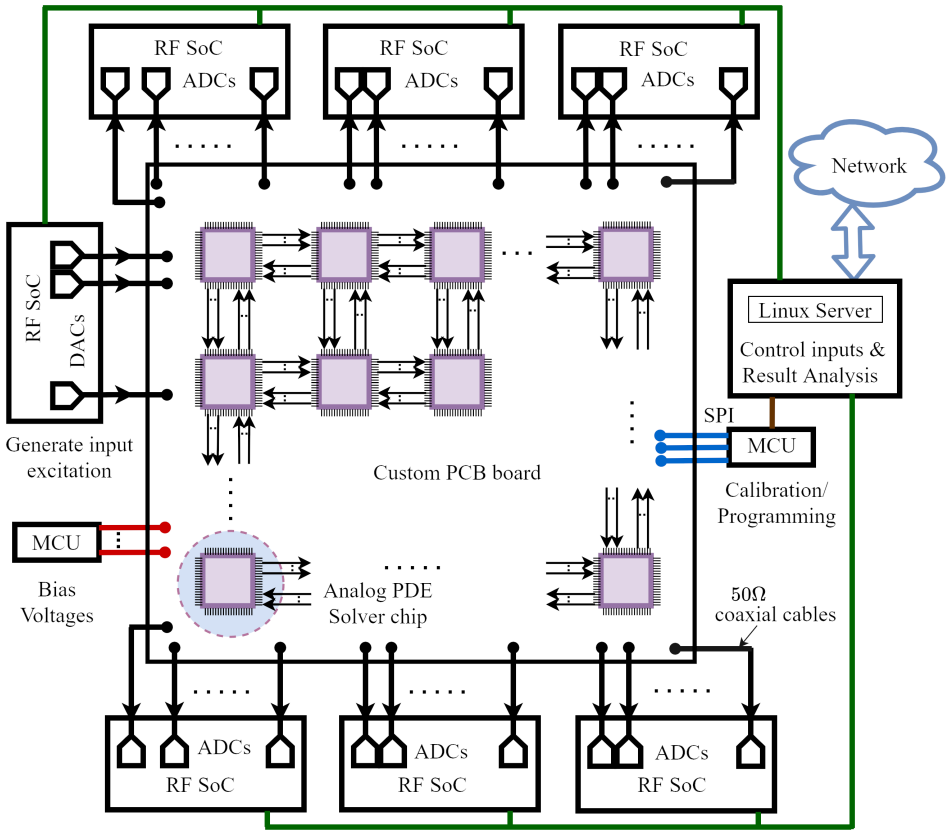
- Explores analog computing concepts, using integrated circuits (IC) technologies, to obtain additional performance from IC platforms.

- Analog computer (AC) is not a general solution to the slowing of Moore's law.
- ACs are a promising for better computational performance in specialized cases.
- ACs find applications across multiple verticals including AI/ML, and scientific computing such as electromagnetic and plasma physics simulations.

Analog Computers for Solving PDEs

- The solutions of PDEs are continuous in time.

Analog Computer for Solving PDEs



- The proposed analog CMOS solver provides a software-reconfigurable general purpose architecture for solving coupled PDEs.
- Boundary conditions, excitations (inputs), computed results (outputs), reconfiguration commands, and calibration signals need to be provided from a series of FPGA boards and ADC/DAC channels.

Continuous-time Algorithms for Solving Maxwell's Equations

Two methods to design analog accelerators for solving electromagnetic equations have been investigated [9].

1. Continuous time in Laplace domain (CTLD) method: The spatial domain partial derivatives are approximated using discrete finite differences, while applying the Laplace transform (LT) along the time dimension [10–13].
2. All-pass delay approximation (APDA) method: The discrete time-difference operators in the standard finite-difference time-domain (FDTD) method (Yee algorithm) are replaced using a continuous-time delay operator (of duration τ), which can be realized efficiently on analog CMOS technology as an active-circuit based analog all-pass filter $\phi(s) = \left(\frac{1-s\tau/2M}{1+s\tau/2M}\right)^M \approx exp(-s\tau)\,, M \in \mathbb{Z}^+$ [14–19].

1-D Analog Maxwell's Equations

Maxwell's Equations

Maxwell's equations in an isotropic source-free region of space can be expressed as [20, 21]

$$\begin{aligned} \nabla \times \mathbf{E} &= -\mu \frac{\partial \mathbf{H}}{\partial t}, \\ \nabla \times \mathbf{H} &= \epsilon \frac{\partial \mathbf{E}}{\partial t}, \end{aligned} \tag{1}$$

where $\mathbf{E} \equiv (E_x, E_y, E_z)$ and $\mathbf{H} \equiv (H_x, H_y, H_z)$.

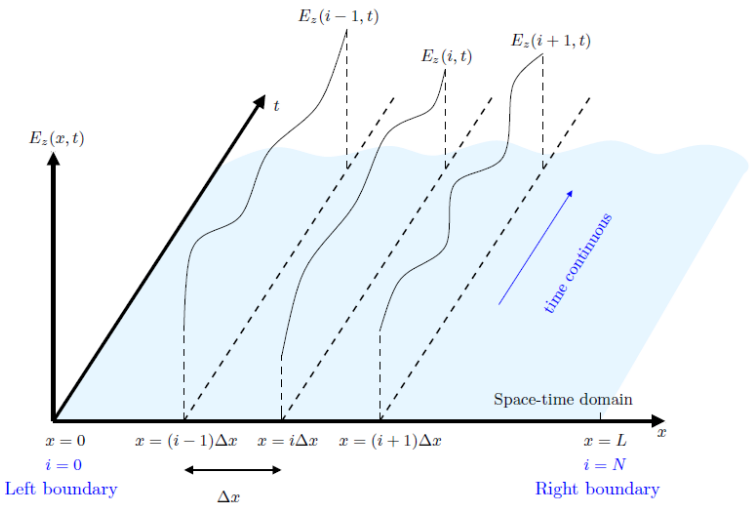
For 1-D, the TM mode electromagnetic fields are described by

$$\begin{aligned} \frac{\partial E_z}{\partial t} &= \frac{1}{\epsilon} \frac{\partial H_y}{\partial x}, \\ \frac{\partial H_y}{\partial t} &= \frac{1}{\mu} \frac{\partial E_z}{\partial x}, \end{aligned} \tag{2}$$

1-D wave equation can be derived as,

$$\frac{1}{c^2} \frac{\partial^2 \mathbf{E_z}}{\partial^2 t} = \frac{\partial^2 \mathbf{E_z}}{\partial^2 x}, \quad c = \frac{1}{\sqrt{\mu\epsilon}} \tag{3}$$

Continuous-time in Laplace Domain (CTLD) Method



1-D Wave Equation

The function $E_z(x,t)$ provides the electric field intensity of a propagating wave at position x and time t. Then, $E_z(x,t)$ satisfies the PDE [20, 21]

$$\frac{1}{c^2}\frac{\partial^2 E_z(x,t)}{\partial t^2} = \frac{\partial^2 E_z(x,t)}{\partial x^2}, \tag{4}$$

where c is the wave speed.

Consider a spatial domain $0 \leq x \leq L$, which is discretized into $N+1$ spatial points, where $\Delta x = \frac{L}{N}$.

Step 1: Approximate the spatial domain partial derivatives using finite differences

$$\left.\frac{\partial^2 E_z(x,t)}{\partial x^2}\right|_{x=i\Delta x} \approx \frac{E_z(i-1,t) - 2E_z(i,t) + E_z(i+1,t)}{\Delta x^2} \tag{5}$$

Analog Wave Equation Solver: CTLD Method

Thus, the resulting expression is

$$\frac{1}{c^2}\frac{\partial^2 E_z(i,t)}{\partial t^2} \approx \frac{E_z(i-1,t) - 2E_z(i,t) + E_z(i+1,t)}{\Delta x^2} \tag{6}$$

Step 2: Apply the Laplace transform along time [12, 13, 22].

$$\frac{1}{c^2}s^2\bar{E}_z(i,s) - sF(i) - G(i) = \frac{\bar{E}_z(i-1,s) - 2\bar{E}_z(i,s) + \bar{E}_z(i+1,s)}{\Delta x^2} \tag{7}$$

Here, $F(i)$ and $G(i)$ define the initial conditions of the system.

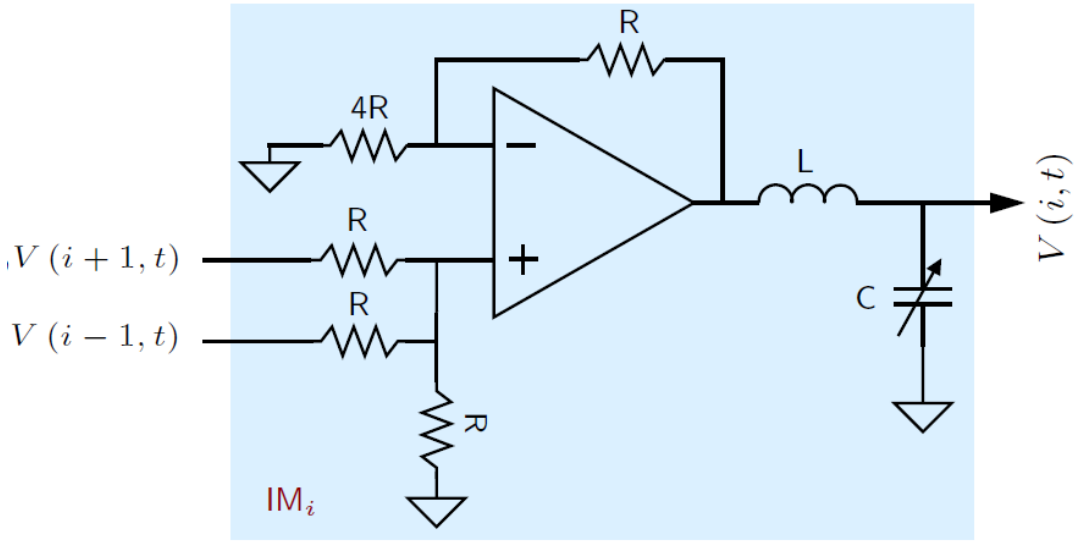
For zero initial conditions, the mixed domain update equation can be obtained as

$$\bar{E}_z(i,s) = \frac{\bar{E}_z(i+1,s) + \bar{E}_z(i-1,s)}{2(As^2+1)}, \tag{8}$$

where $A = \frac{\Delta x^2}{2c^2}$ (for internal spatial points).

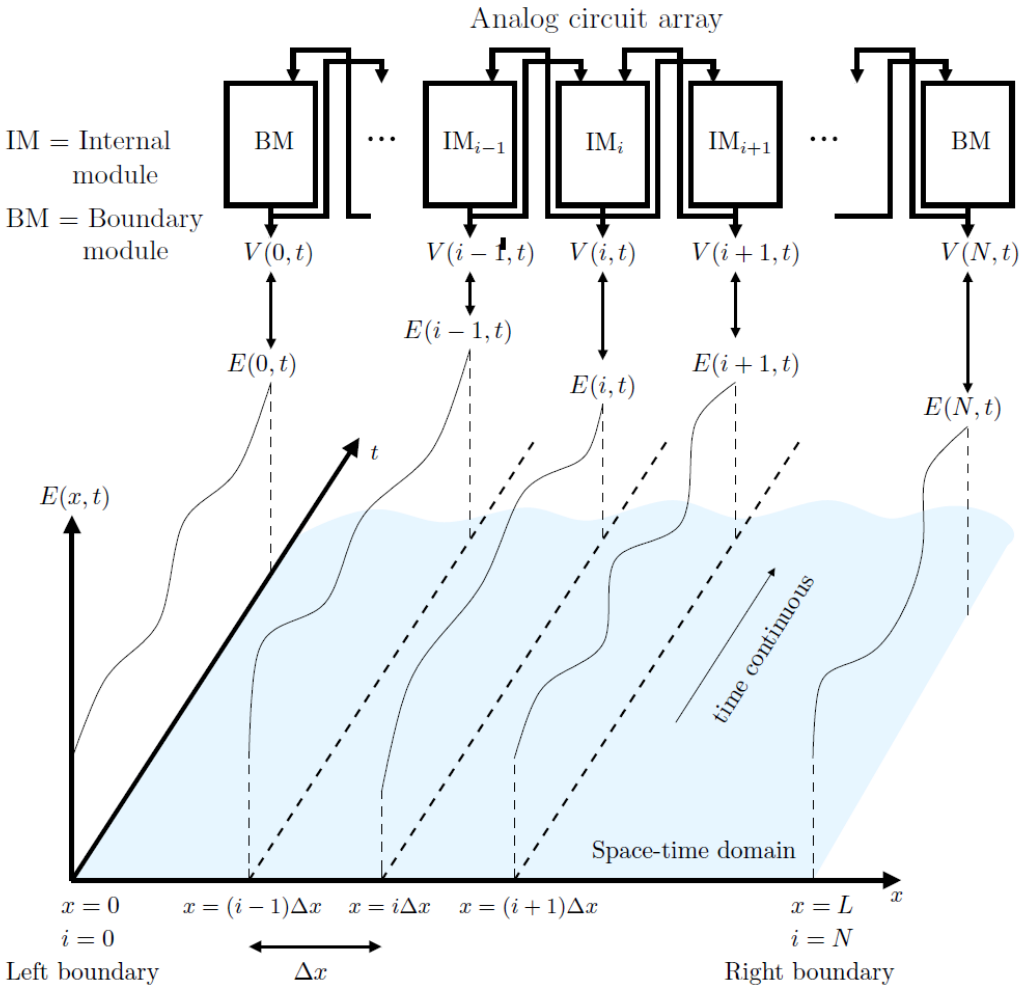
Analog Wave Equation Solver: CTLD Method

$$\bar{E}_z(i,s) = \frac{\bar{E}_z(i+1,s) + \bar{E}_z(i-1,s)}{2(As^2+1)},$$



- The electric field intensity is represented using voltages.
- Scaling and summing operations can be realized op-amp circuits.
- The $\frac{1}{As^2+1}$ operation can be implemented using an LC circuit.
- The continuous-time solution over the whole spatial domain is computed by inter-connecting the IMs in a systolic array architecture.

Analog Wave Equation Solver: CTLD Method



- The continuous-time solution over the whole spatial domain is computed by interconnecting the IMs in a systolic array architecture.

APDA Method for Solving Wave Equation

- Step 1: Approximate the spatial derivatives using finite differences.
- Step 2: In contrast to CTLD method, time domain partial derivatives are approximated using finite differences, while keeping the time variable (τ) continuous

$$\frac{\partial^2 E_z(i,t)}{\partial t^2} \approx \frac{E_z(i,t) - 2E_z(i,t-\tau) + E_z(i,t-2\tau)}{\tau^2}, \tag{9}$$

- Thus, the wave equation can be expressed as

$$\begin{aligned} &\frac{E_z(i,t) - 2E_z(i,t-\tau) + E_z(i,t-2\tau)}{(c\tau)^2} = \\ &\frac{E_z(i-1,t-\tau) - 2E_z(i,t-\tau) + E_z(i+1,t-\tau)}{\Delta x^2} \end{aligned} \tag{10}$$

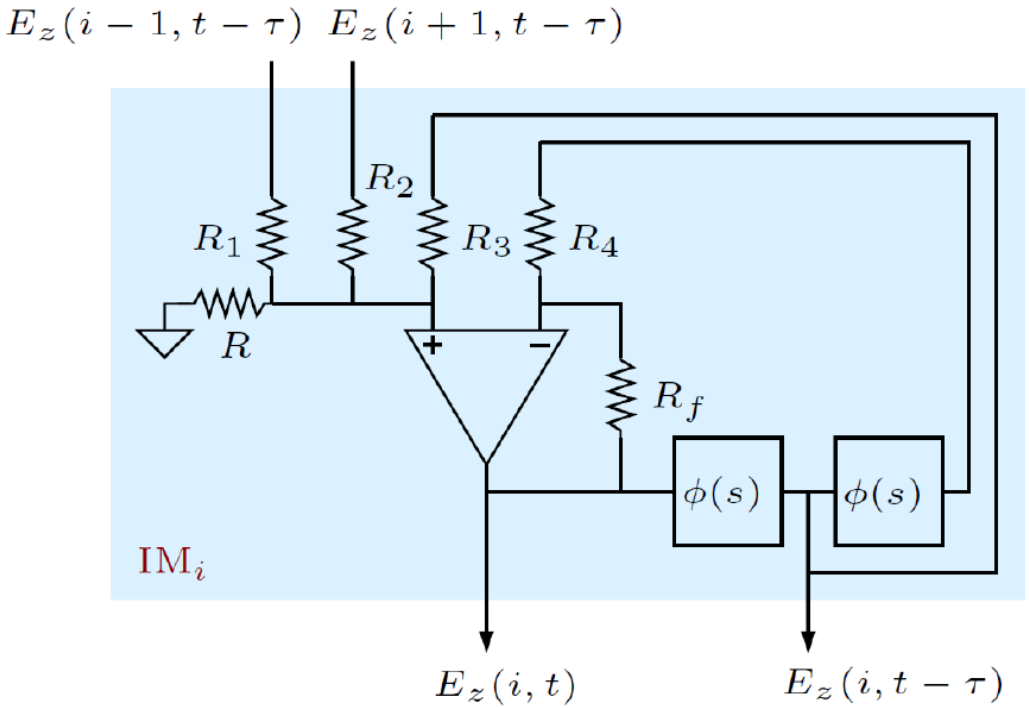
- Step 3: Application of the Laplace transform along the time dimension (with zero initial conditions) leads to [14–19]

$$\begin{aligned} \bar{E}_z(i,s) &= K^2 \left[\bar{E}_z(i+1,s) + \bar{E}_z(i-1,s)\right] e^{-s\tau} \\ &+ 2\left(1-K^2\right)\bar{E}_z(i,s)\, e^{-s\tau} - \bar{E}_z(i,s)\, e^{-2s\tau}, \end{aligned} \tag{11}$$

where $K = \frac{c\tau}{\Delta x} \leq 1$.

APDA Method for Solving Wave Equation

- Equation (11) can be implemented using the below circuit.



- Summing and scaling operations are realized using op-amps.
- The continuous-time delay operator $e^{-s\tau}$ is approximated using an analog all-pass filter, which has an approximate s-domain transfer function $e^{-s\tau}$, where τ is the group delay of the all-pass filter.
- Replace the digital delays (z_t^{-1} in the z-domain transfer function) in the FDTD method using analog all-pass filters.

Comparative Analysis of the Analog Wave Equation Solver

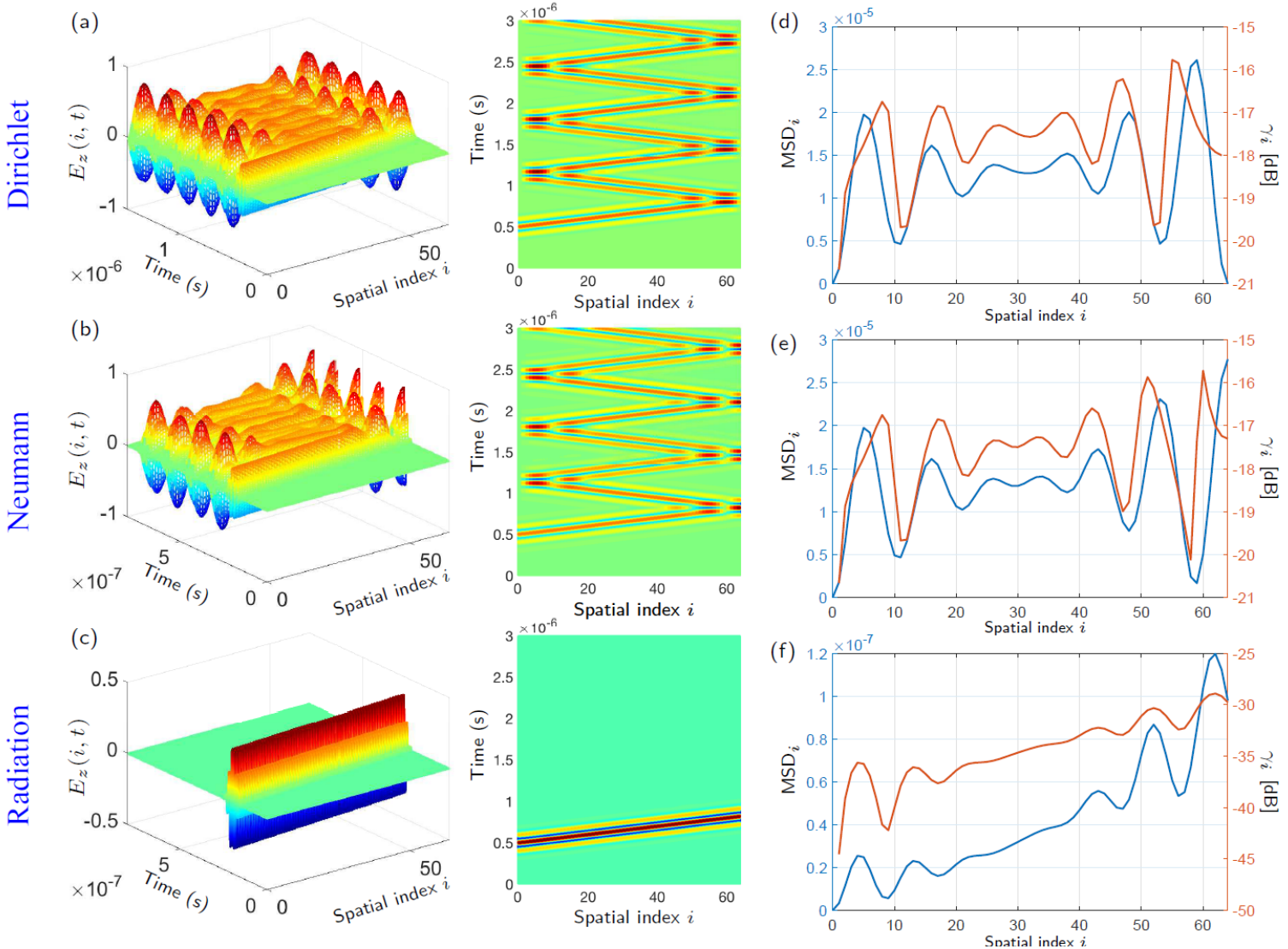
- In order to quantify how much our continuous-time solution deviates from the standard FDTD solution, the mean squared difference (MSD) between the two solutions and the noise energy to signal energy ratio γ (in dB) have been calculated.
- An FDTD-based wave equation solver is implemented using MATLAB.
- The MSD_i for the electric field solution is defined as

$$\text{MSD}_i = \frac{1}{N_t} \sum_{n=0}^{N_t-1} \left[E_F\left(i, n\Delta T\right) - E_A\left(i, t\right) \right]^2, \tag{12}$$

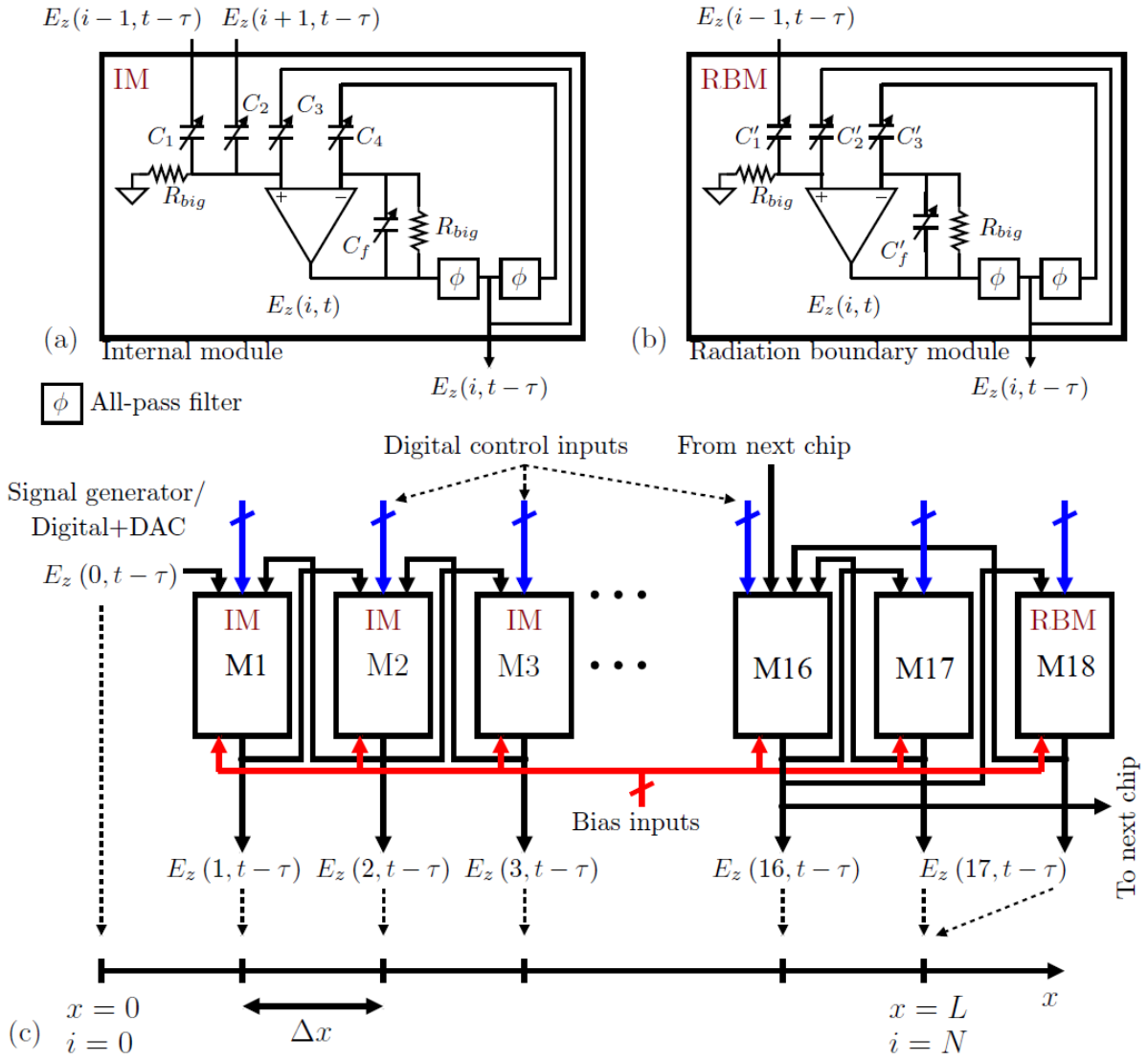
  where $E_F\left(i, n\Delta T\right)$ and $E_A\left(i, t\right)$ are the solutions of the FDTD and the proposed analog solvers, respectively ($t = n\Delta T$).
- The γ_i is expressed as

$$\gamma_i = 10 \log_{10} \frac{\sum_{n=0}^{N_t-1} \left[E_F\left(i, n\Delta T\right) - E_A\left(i, t\right) \right]^2}{\sum_{n=0}^{N_t-1} E_F\left(i, n\Delta T\right)^2}. \tag{13}$$

Comparative Analysis of the Analog Wave Equation Solver

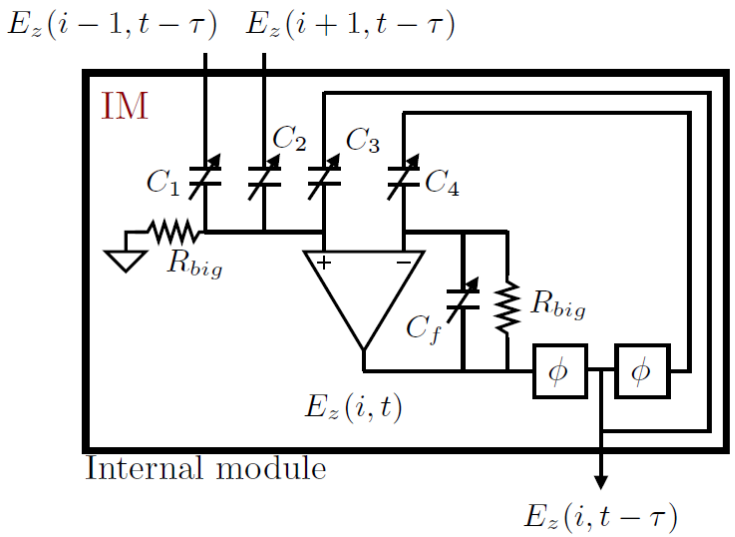


Top-level Block Diagram of the Analog Computer for Solving Wave Equation



CMOS Design of the 1-D Wave Equation Solver

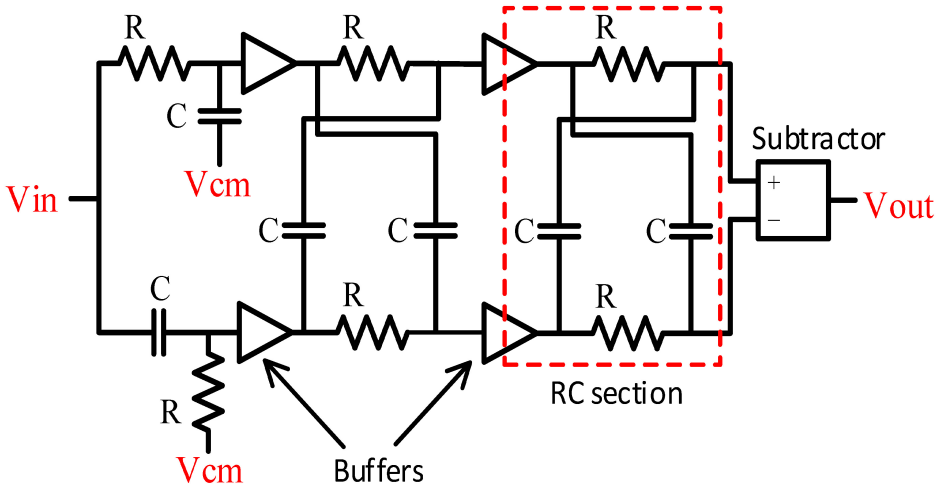
- The circuit designs employed the TSMC analog CMOS library with the 0.18 micrometer process. Cadence integrated circuit design software is used to design the proposed AC.
- The analog bandwidth $F_{compute}$ for CT operations of the AC is set to 50 MHz. This results a minimum wavelength of $\lambda_{min} = \frac{c}{F_{compute}}$.
- The spatial step size is set to $\Delta x = \frac{\lambda_{min}}{8}$.
- τ is selected as 1.6 ns to satisfy the stability condition $\tau \leq \frac{\Delta x}{c} = 2.5$ ns. Thus, the equivalent temporal update rate in the AC is 625 MHz.



Op-amp gain bandwidth product > 500 MHz

All-pass filter gain and propagation delay (1-2 ns) should be constant over 50 MHz

CMOS All-pass Filter Design

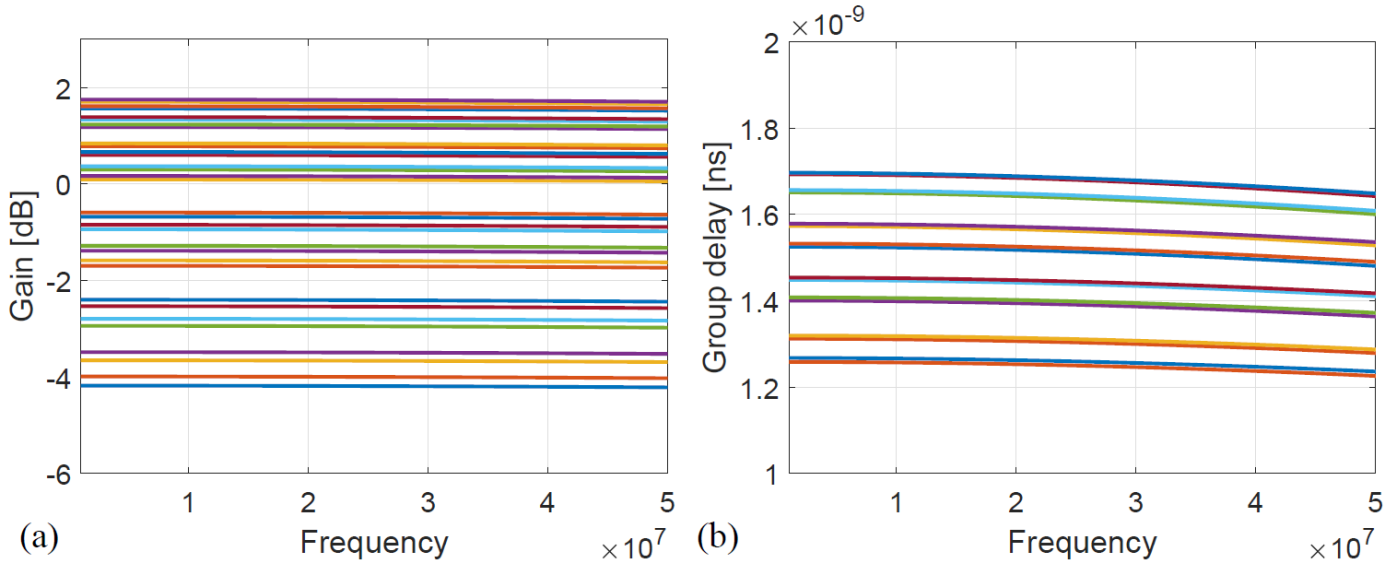


- The Laplace domain representations $e^{-s\tau}$ in the update equations are approximated as $e^{-s\tau} \approx \left[\frac{1-\frac{s\tau}{2M}}{1+\frac{s\tau}{2M}}\right]^M$, and is realized using a cascade of M first-order all-pass filters.
- Typically, $M = 3$ is sufficient for approximation of τ [19].
- The complete transfer function of the system can be obtained as

$$\frac{V_{out}(s)}{V_{in}(s)} = \phi(s) = \left(\frac{1-RCs}{1+RCs}\right)^3 = \left(\frac{1-\frac{j\omega\tau}{6}}{1+\frac{j\omega\tau}{6}}\right)^3, \tag{14}$$

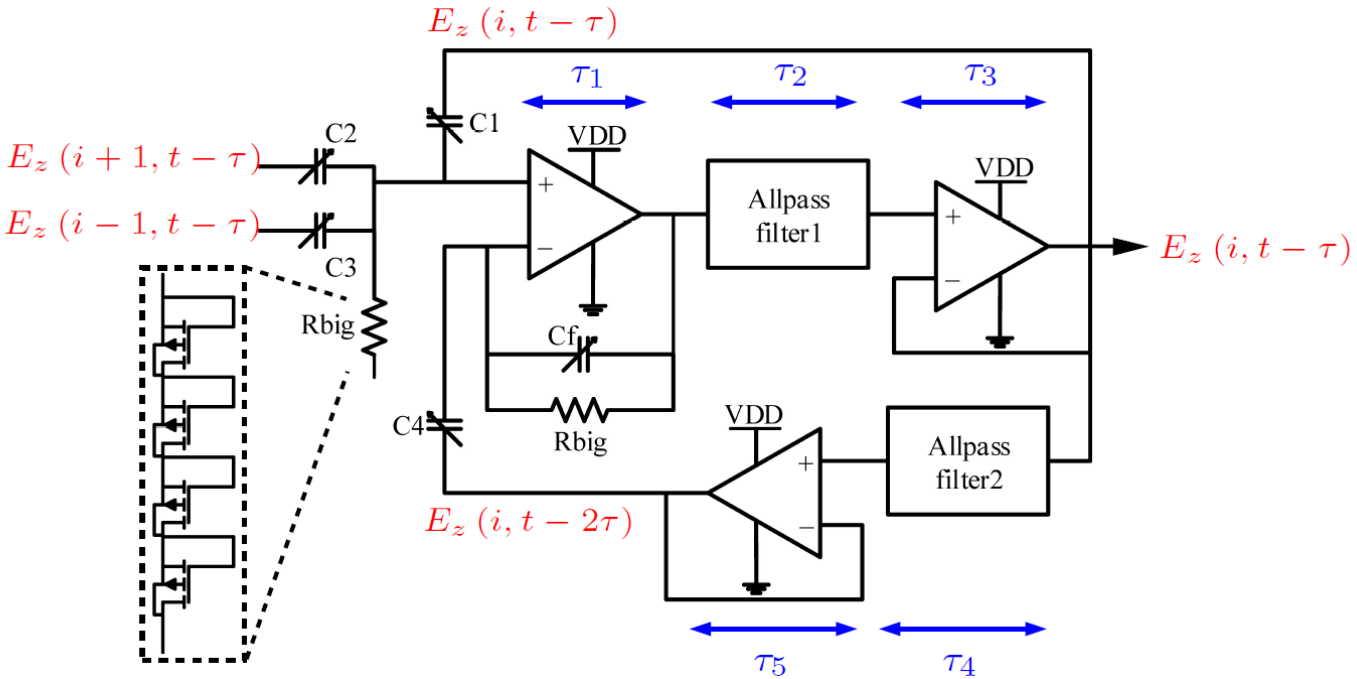
The group delay of the all-pass filter is $\tau = 6RC$.

CMOS All-pass Filter Design



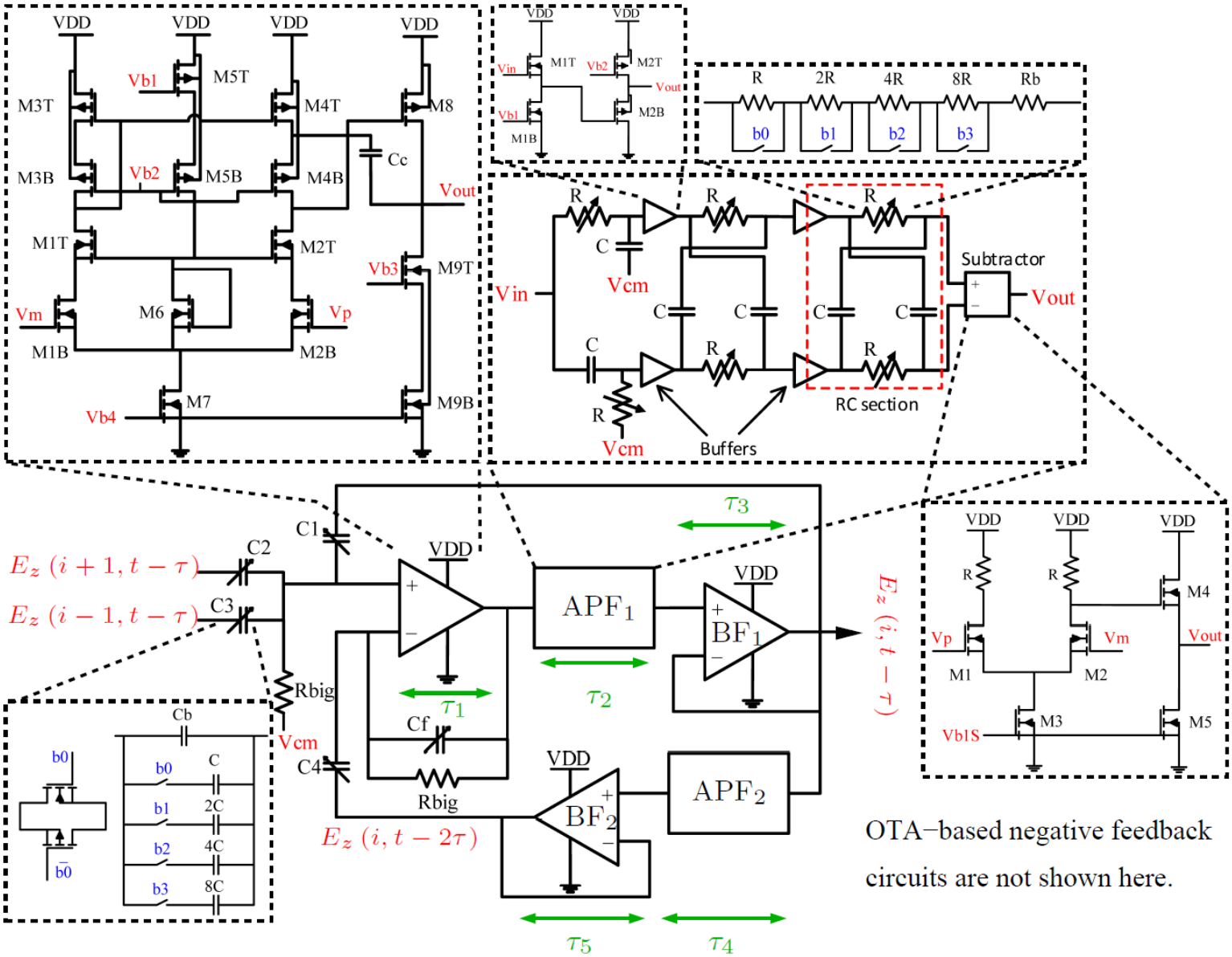
- The gain of all-pass filter is tunable (from -4 dB to 2 dB). A binary weighted resistor DAC is utilized in the subtractor to tune the gain.
- Resistors in the RC section of all-pass filter are replaced using resistor DACs to tune the propagation delay (from 1.2 ns to 1.7 ns).
- The tunablity of the all-pass filter is important for calibration and compensating PVT variations.

CMOS Implementation of the Internal Module



- Resistors Rbig are used to DC bias the op-amp. They are implemented as pseudo resistors.
- Accurate implementation of the continuous-time delay operator τ is an important task of the designing process.
- Here, the continuous-time delay operator $\tau = \tau_1 + \tau_2 + \tau_3$. The signal at the output of the buffer can be denoted as $E_z(i, t-\tau)$.
- The group delay τ_4 is configured such that $\tau_4 = \tau - \tau_5$.

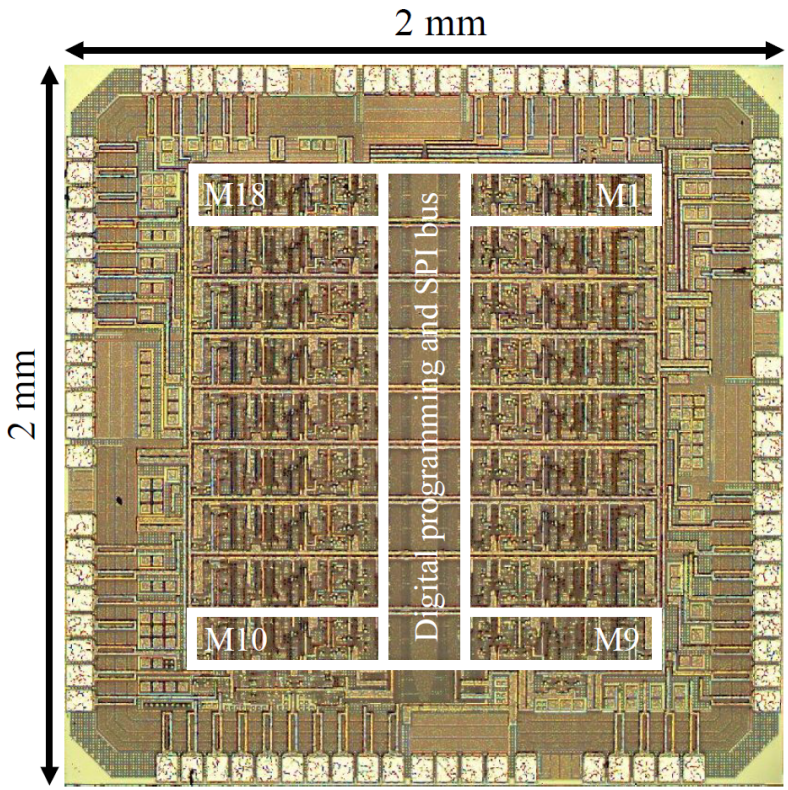
CMOS Implementation of the Internal Module



OTA–based negative feedback circuits are not shown here.

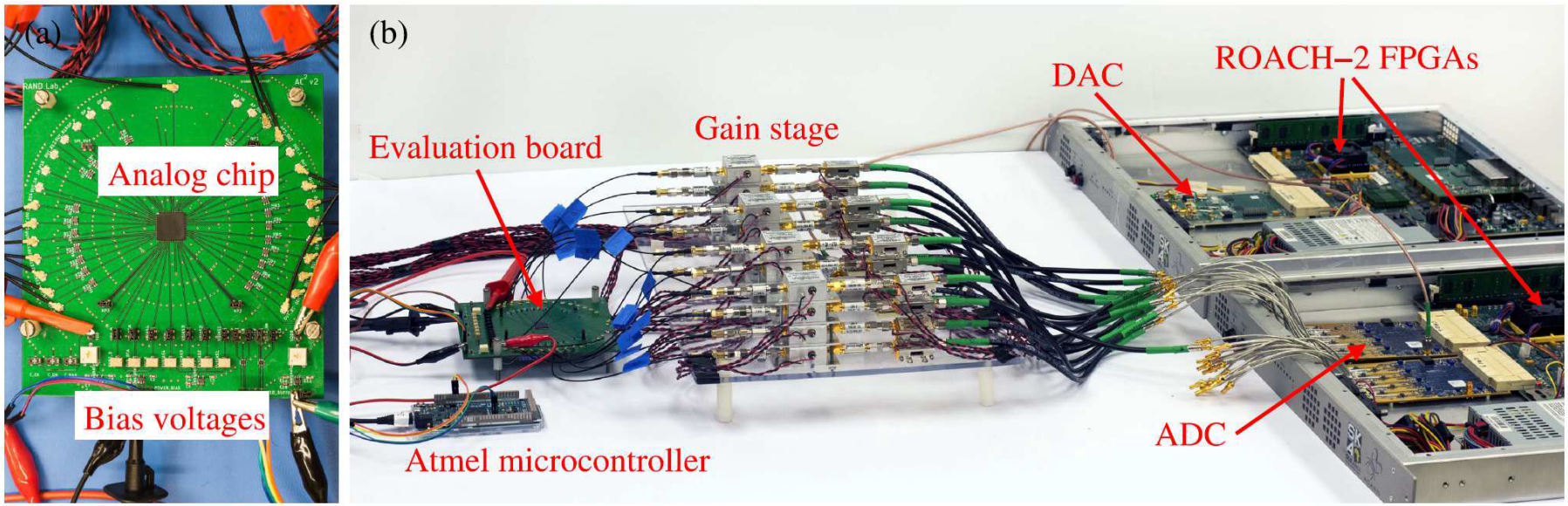
Analog Computer for Solving 1-D Wave Equation

- 30MHz of analog bandwidth.
- 200mW of power.
- 16 internal modules.
- Digitally-programmable boundaries.
- Digital calibration.
- Capable of cascading chips.



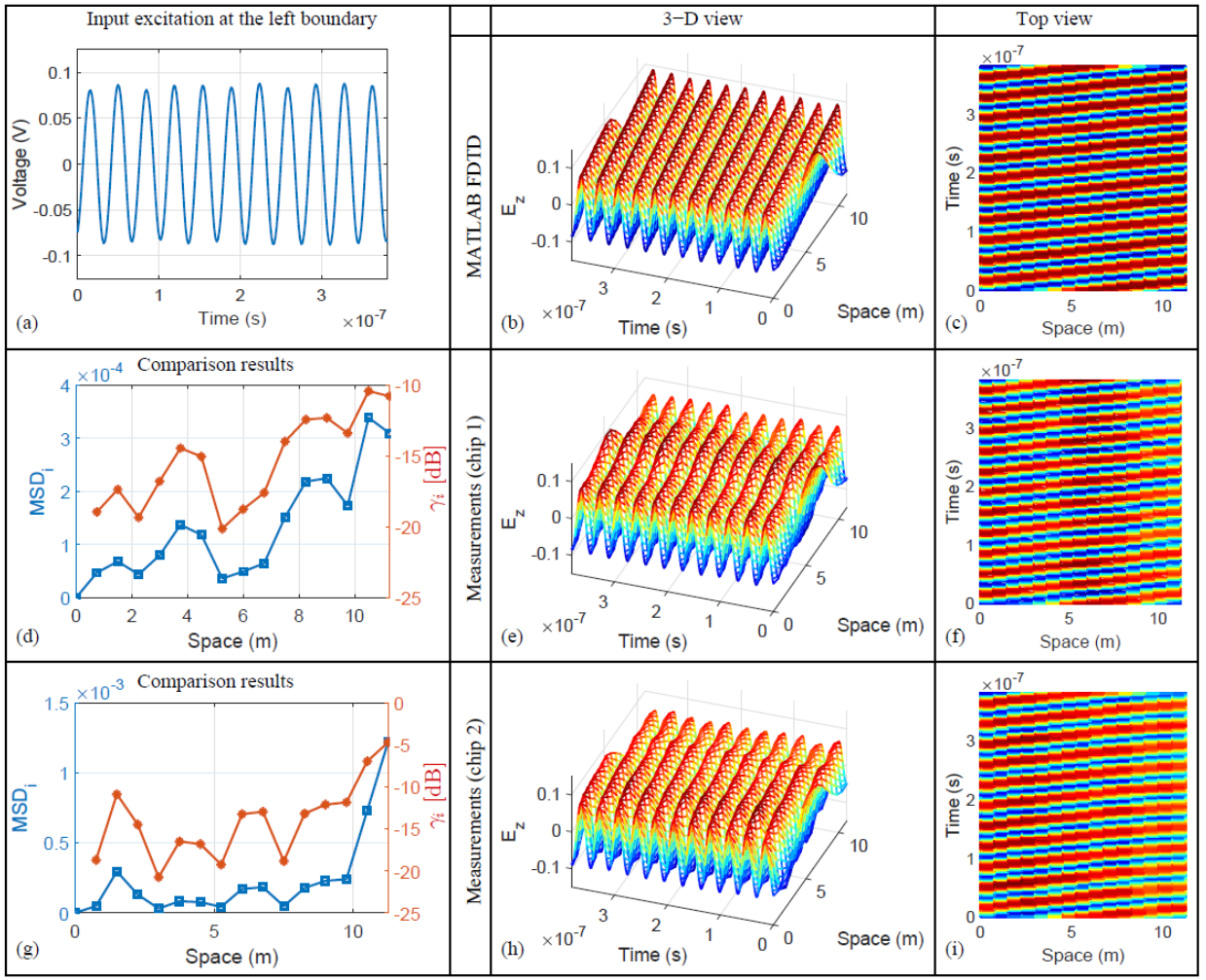
N. Udayanga et al., "A Radio Frequency Analog Computer for Computational Electromagnetics," in IEEE Journal of Solid-State Circuits, vol. 56, no. 2, pp. 440-454, Feb. 2021

Analog-digital Hybrid Measurement Setup



- Input excitations and boundary conditions are generated inside a ROACH-2 FPGA and supplied to the analog chip through a digital-to-analog converter (DAC) board (DAC2x1000-16).
- Computed analog solutions (computational outputs of the analog chip) are routed back into the FPGA through a 16-input analog-to-digital converter (ADC) board (ADC16x250-8).

Accuracy: Measurements vs MATLAB FDTD



- The means squared error percentage is 1%-10% (depending on the spatial location).

N. Udayanga et al., "A Radio Frequency Analog Computer for Computational Electromagnetics," in IEEE Journal of Solid-State Circuits, vol. 56, no. 2, pp. 440-454, Feb. 2021

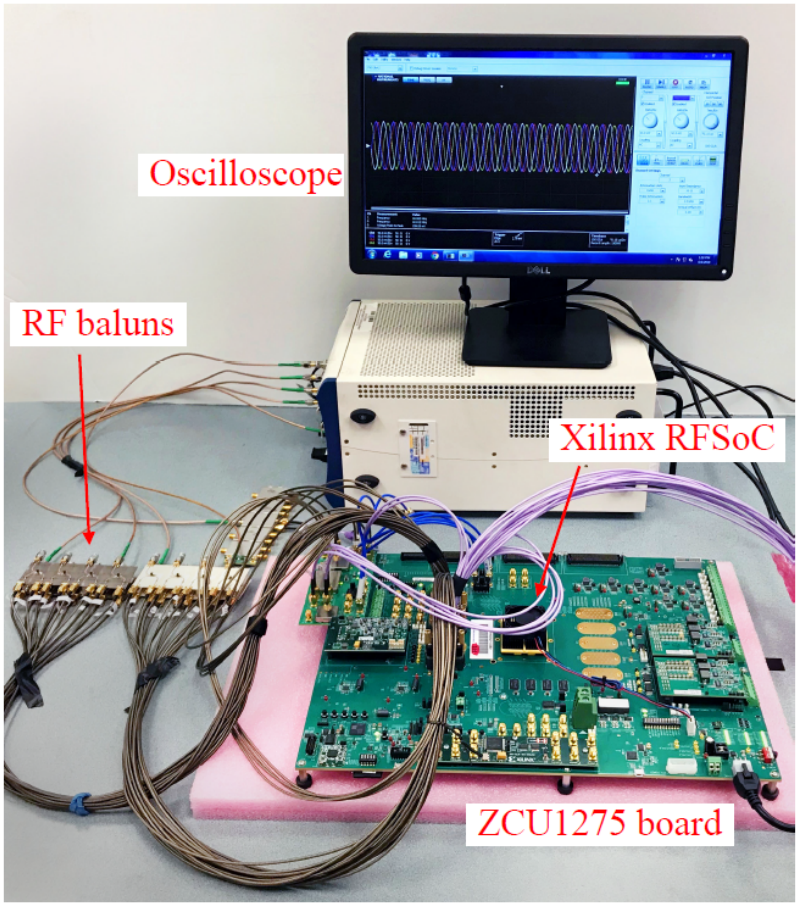
Estimating the Speed-up

Input signal is 30 MHz sinusoidal signal with a sample period of 1.6 ns	**Our chip**	CUDA C FDTD[1] design running on NVIDIA GeForce GTX 1080 Ti GPU	Computer with two Intel Xeon Silver 4110 CPU @ 2.10GHz, 8 Core(s), and 256 GB of RAM	
			FDTD MATLAB code	FDTD C code[1]
Time to simulate 1 ms of physical time	**1 ms**	420 ms	99 ms	26 ms
Time to simulate 10 ms of physical time	**10 ms**	4230 ms	984 ms	261 ms
Time to simulate 100 ms of physical time	**100 ms**	42500 ms	10075 ms	2506 ms
Time to simulate 1000 ms of physical time	**1000 ms**	423400 ms	101589 ms	27009 ms
Average speedup		**420**×	**100**×	**26**×

- The AC is 420× faster when compared to the NVIDIA GeForce GPU.
- The estimated speedup of the AC is about 100× and 26× compared to the MATLAB- and C-based FDTD solvers, respectively.

[1] C-codes was developed by Ocius employee Nathaniel Hawk.

Estimating the Speedup



Input signal is 30 MHz sinusoidal signal with a sample period of 1.6 ns	Our chip	FDTD FPGA design running on xczu29dr-ffvf1760 RFSoC @222 MHz
Time to simulate 1 ms of physical time	1 ms	2.8 ms
Time to simulate 10 ms of physical time	10 ms	28 ms
Time to simulate 100 ms of physical time	100 ms	280 ms
Time to simulate 1000 ms of physical time	1000 ms	2800 ms
Average speedup		2.8×
$F_{compute}$/Power	**0.15 MHz/mW**	0.01 MHz/mW

An FPGA-based FDTD solver is implemented on Xilinx RF system on chip (SoC) (xczu29dr-ffvf1760) using the ZCU1275 board and clocked at 222MHz with about 900mW of dynamic power (excluding ADC and DACs). The corresponding speedup of the 180nm CMOS AC is 2.8× at 200mW.

Continuous-time Algorithms for Solving Nonlinear PDEs

- Starting with a standard numerical scheme that can solve nonlinear PDEs continuous-time update equations are obtained using the APDA method.
- Consider 1-D system with two conservative variables $u_1(x,t)$ and $u_2(x,t)$ with $0 \leq x \leq L_x$, and the spatial step size $\Delta x = \frac{L_x}{N_x}$. Here, $i \in \{0, 1, \ldots, N_x\}$ is the spatial index.

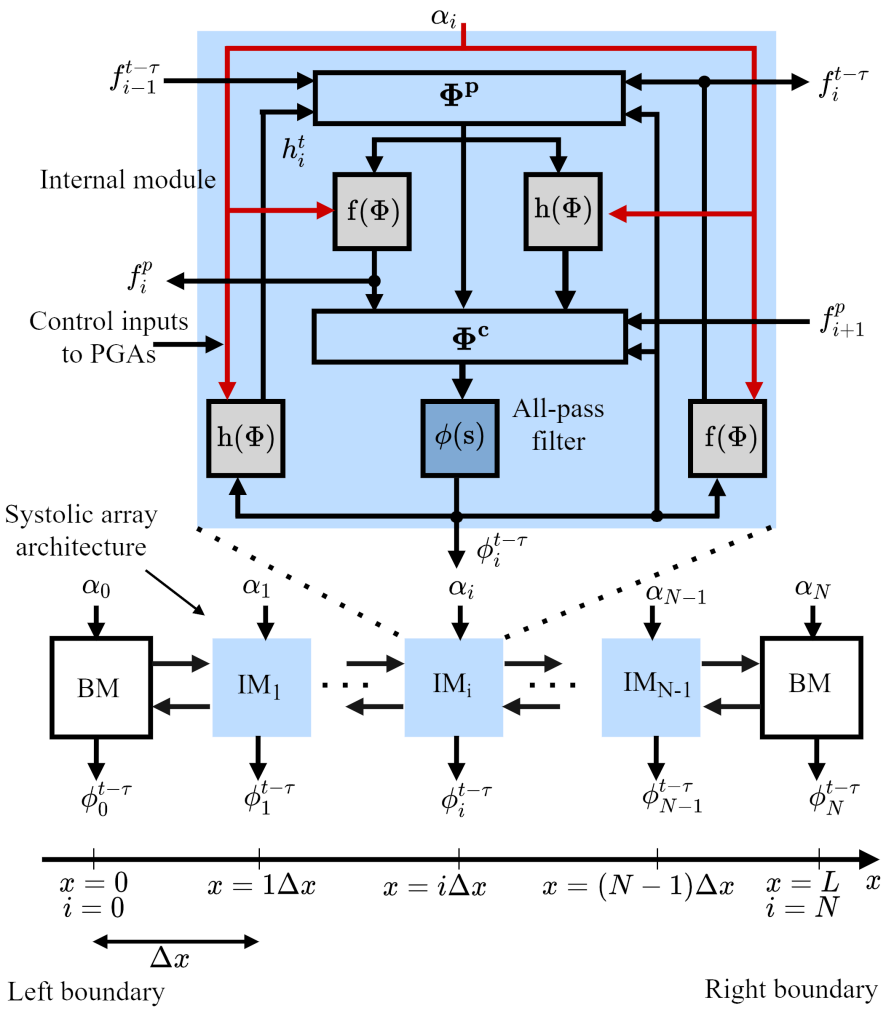
Let $\Phi_i^t = \begin{bmatrix} u_1(i,t) \\ u_2(i,t) \end{bmatrix}$, $f_i^t = \begin{bmatrix} f_1\left(\Phi_i^t\right) \\ f_2\left(\Phi_i^t\right) \end{bmatrix}$, and $h_i^t = \begin{bmatrix} h_1\left(\Phi_i^t\right) \\ h_2\left(\Phi_i^t\right) \end{bmatrix}$, where Φ is a vector with two variables u_1, u_2. f and h are the flux term and source term of Φ, respectively.

Then we can state the two step continuous-time MacCormack's scheme [23–25] as

$$\begin{aligned} \Phi_i^p &= \Phi_i^{t-\tau} - c_0 \frac{\tau}{\Delta x}\left(f_i^{t-\tau} - f_{i-1}^{t-\tau}\right) + \tau h_i^{t-\tau}, \\ \Phi_i^t &= \frac{1}{2}\left(\Phi_i^{t-\tau} + \Phi_i^p\right) - c_0 \frac{\tau}{2\Delta x}\left(f_{i+1}^p - f_i^p\right) + \frac{\tau}{2} h_i^p. \end{aligned} \tag{15}$$

Here, superscript p denotes the predictor step.

Analog Computing Architecture

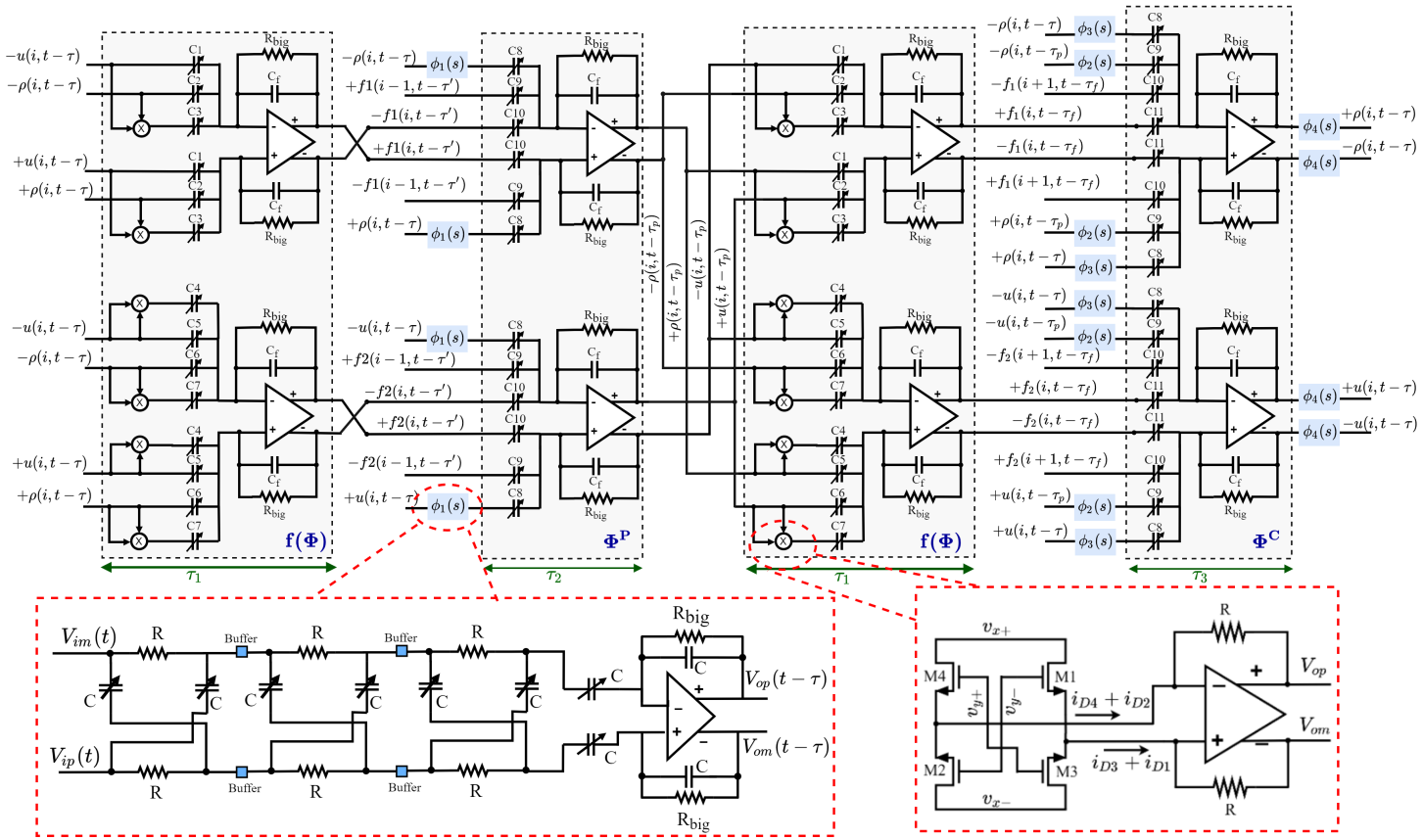


- SDTC equations are mapped into circuits.
- Internal modules (IMs) compute Φ_i^t at spatial points $i \in \{1, 2..., N-1\}$.
- At the boundaries $i = 0$ and $i = N$, $f_{-1}^{t-\tau} = 2f_0^{t-\tau} - f_1^{t-\tau}$ and $f_{N+1}^p = 2f_N^p - f_{N-1}^p$, respectively.
- Flux term f is in the form

$$f_1(u_1, u_2) = \sum_{k_1=0}^{N_1} \sum_{k_2=0}^{N_2} \alpha_{k_1,k_2} u_1^{k_1} u_2^{k_2}.$$

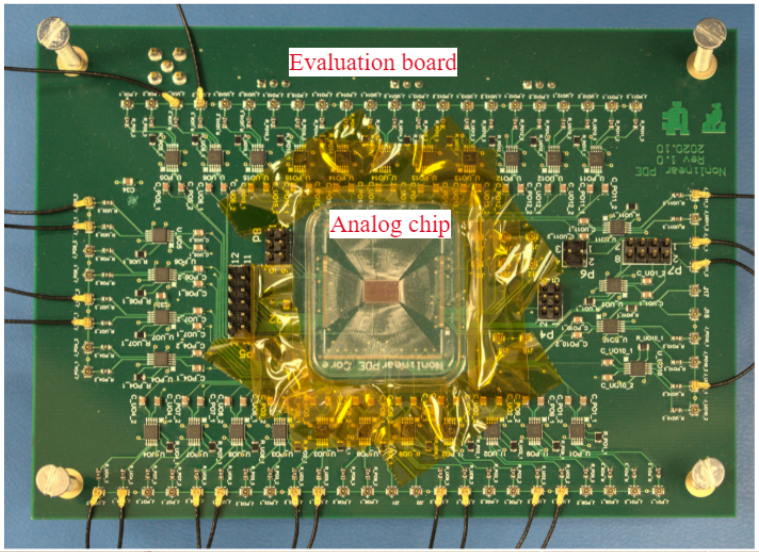
Nonlinear PDE solving IC for Acoustic Wave Equation

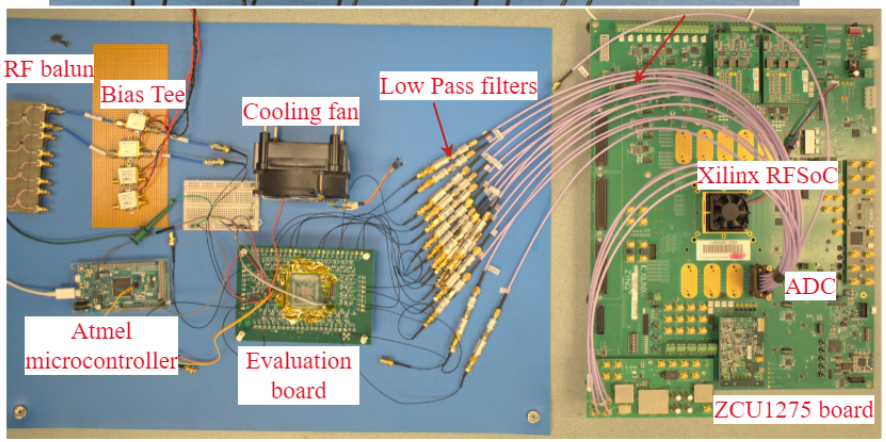
- A prototype IC was fabricated to solve the acoustic shock wave tube problem.



H. Malavipathirana et al.,"A Fast and Fully Parallel Analog CMOS Solver for Nonlinear PDEs," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 8, pp. 3363-3376, Aug.2021

Nonlinear PDE solving IC for Acoustic Wave Equation





- The analog solver models the propagation of acoustic waves along a variable area duct and computes the acoustic flow velocity and density at 15 spatial grid points.
- Chip consists of 450 op-amps with a gain bandwidth product of 650 MHz.
- This IC was designed using TSMC 180 nm CMOS technology and operates at 1.8 V.

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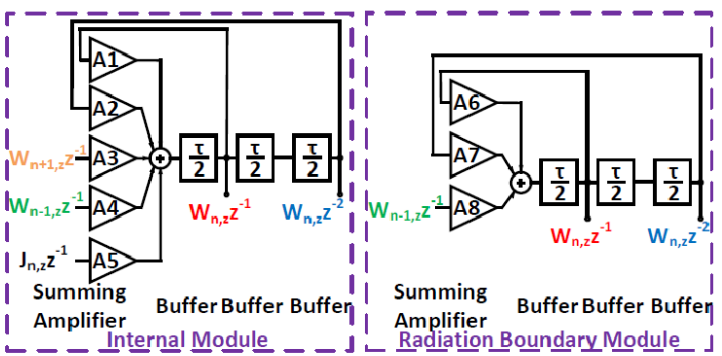
Discrete-Time Analog Computer for Solving 1-D Wave Equation

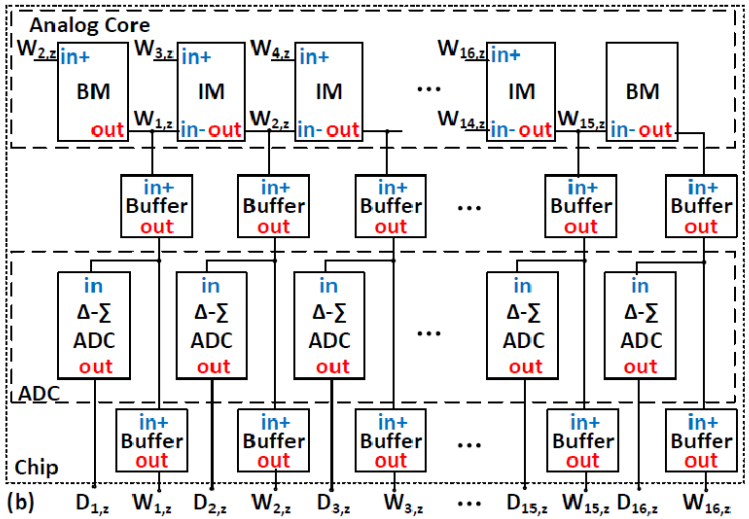
- Continuous-time AC has higher computational bandwidth, but requires significant off-line calibration to improve solution accuracy.
- Continuous-time AC requires realization of time delays using on-chip *RC* products, which are sensitive to mismatch an process variations [26].
- Discrete-time (DT) circuits provide an attractive solution, since time delays are directly referenced to a stable clock.
- In DT method, switched-capacitor (SC) based analog circuits can be used to realize transfer functions that depend only on capacitor ratios, which are more accurate.
- DT circuit techniques such as auto-zeroing and correlated double sampling are used to compensate for op-amp imperfections [27].

DT Wave Equation Solver Internal Module



(a)

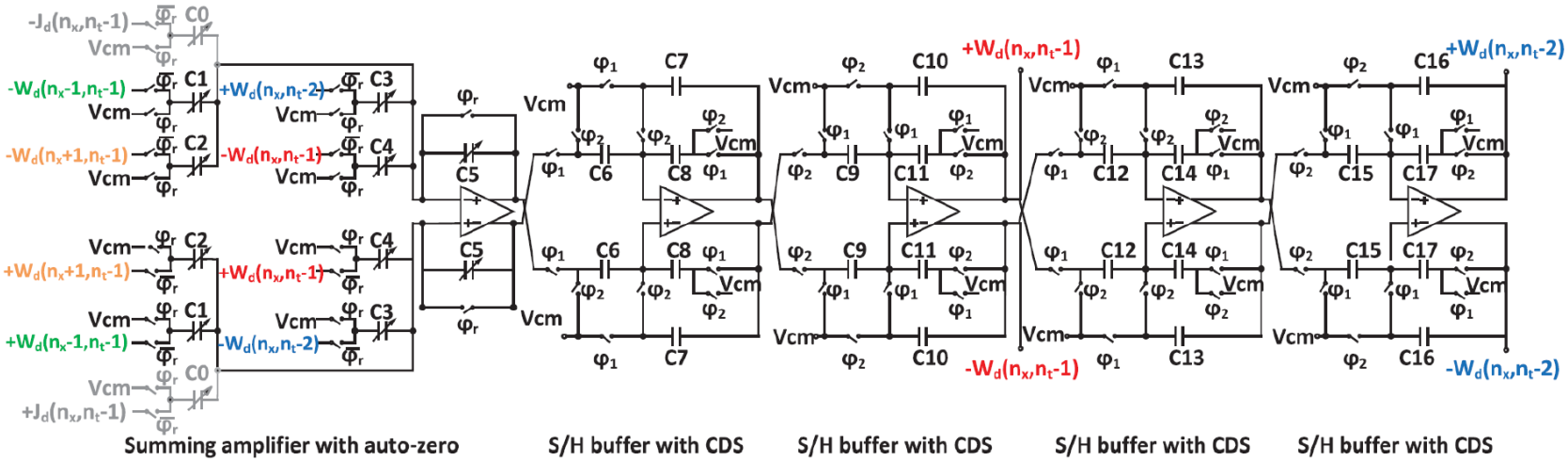
	A1	A2	A3	A4	A5	A6	A7	A8
Generalized 1-D Wave Equation	$\frac{2k_1^2-2}{k_1^2+k_2^2}$	$\frac{k_2^2-k_1^2}{k_1^2+k_2^2}$	$\frac{1}{k_1^2+k_2^2}$	$\frac{1}{k_1^2+k_2^2}$	$\frac{1}{k_1^2+k_2^2}$	$\frac{2k_1^2-2}{k_1^2+k_1}$	$\frac{k_1-k_1^2}{k_1^2+k_1}$	$\frac{2}{k_1^2+k_1}$
1-D Wave Equation	$\frac{2k_1^2-2}{k_1^2}$	-1	$\frac{1}{k_1^2}$	$\frac{1}{k_1^2}$	$\frac{1}{k_1^2}$			



- An internal module computes the wave amplitude at a specific grid position n_x.
- DT wave equation solving AC is capable of solving the generalized wave equation with local input sources and lossy propagation.
- This IC allows selectable boundary conditions, including Dirichlet, Neumann, and radiation boundaries.

J. Liang et al., "An Offset-Cancelling Discrete-Time Analog Computer for Solving 1-D Wave Equations," in IEEE Journal of Solid-State Circuits, vol. 56, no. 9, pp. 2881-2894, Sept. 2021

Schematic of an Internal Module



- AC-coupled summing amplifier is used as the first stage in each module.
- Auto-zero switch (with initial reset signal ψ_r) is used to remove op-amp offset and reset to common mode voltage V_{CM}.
- S/H buffers are utilized to precisely generate a half-clock-cycle delay, $\Delta t/2 = \frac{1}{2f_{clk}}$.

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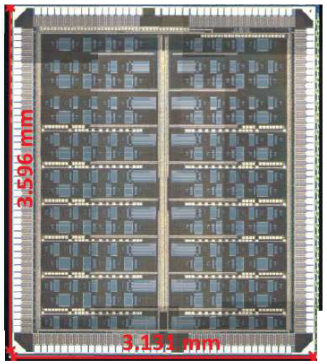
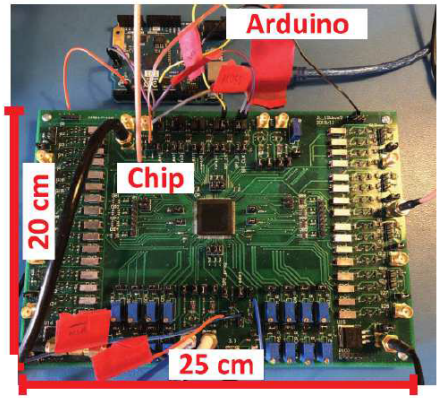
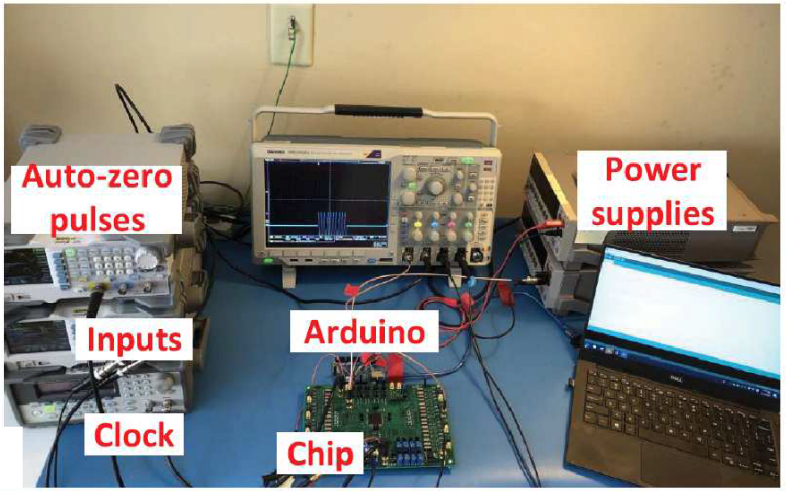
Measurement Setup







- The DT wave equation solving IC was fabricated using TSMC 180 nm process with die area $3.59\ mm \times 3.13\ mm$.
- The chip provides analog outputs as well as digital outputs via on-chip $\Delta - \Sigma$ ADCs.
- Arduino microcontroller is utilized to program the chip through a SPI bus to determine the boundary conditions, location of external excitation, and wave propagation speed.

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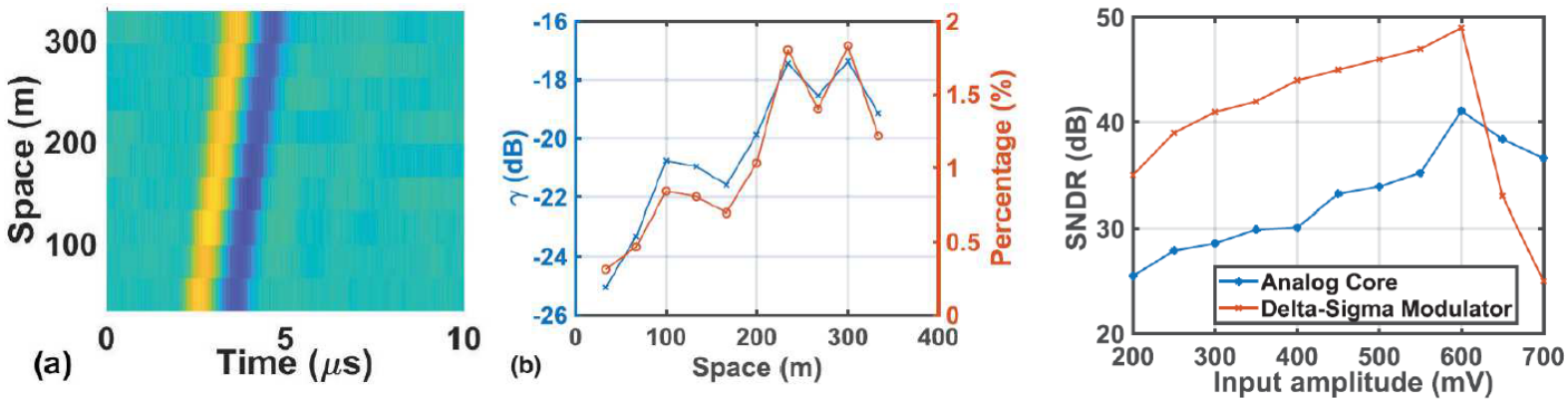
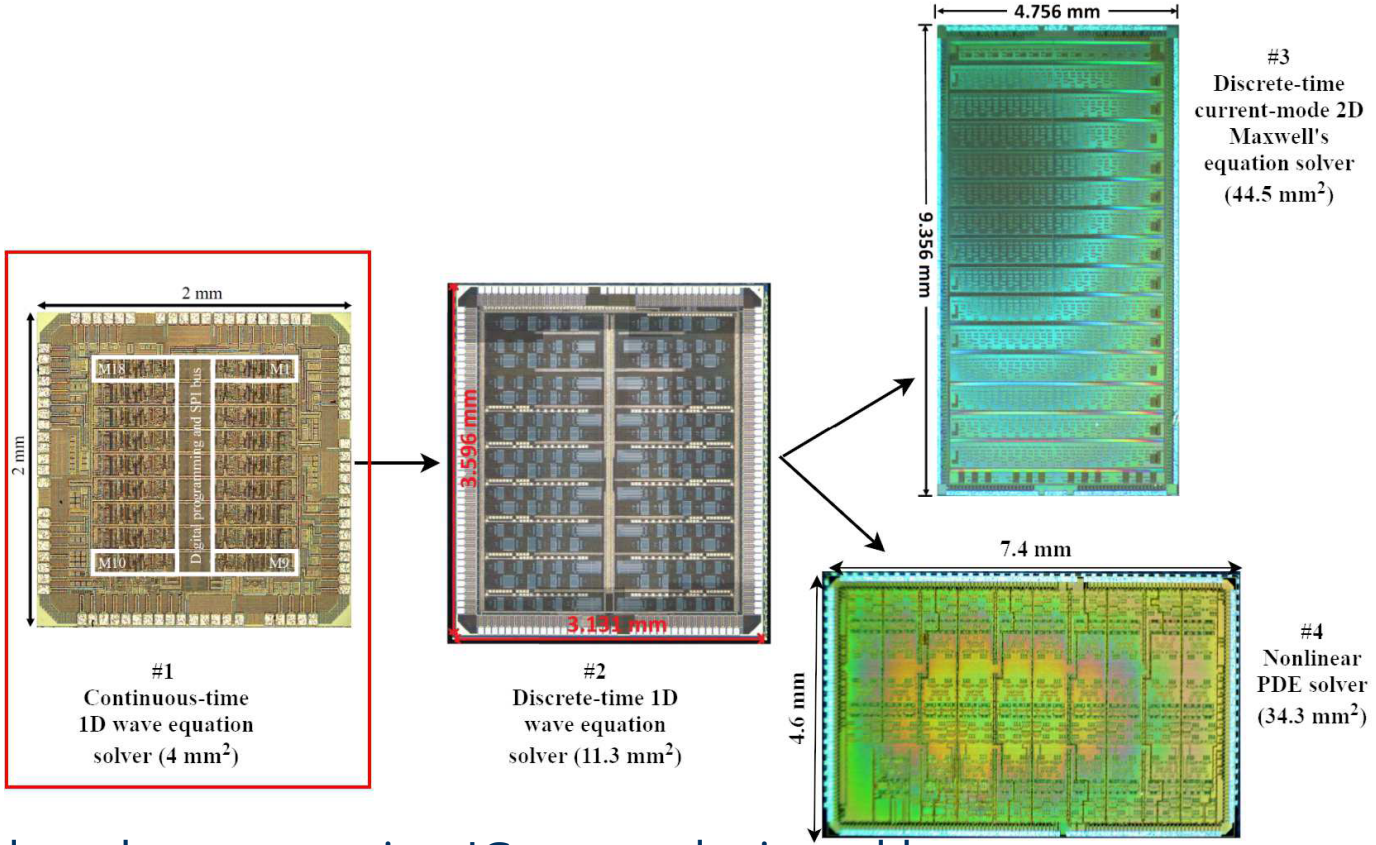
Measurement Results



- This figure shows the measured outputs from the solver with radiation boundary and 0.5 MHz input excitation for a clock frequency of 10 MHz.
- Noise energy to signal energy ratio, γ is -20.4 dB on average (improved accuracy compared to CT solver [28]).
- Peak SNDR of the analog solver is 41 dB and that of the $\Delta - \Sigma$ modulators is 49 dB.
- DT wave equation solver has a computational bandwidth of 2.5 MHz without ADCs and 0.25 MHz bandwidth with ADCs.
- This chip operates at 2.2 V and consumes 560 mW of power.

J. Liang et al., "An Offset-Cancelling Discrete-Time Analog Computer for Solving 1-D Wave Equations," in IEEE Journal of Solid-State Circuits, vol. 56, no. 9, pp. 2881-2894, Sept. 2021

Analog Computing ICs by Our Team



- Several analog computing ICs were designed by our team as part of a DARPA sponsored project.
- Continuous-time wave equation solver (chip #1) [29] and discrete-time wave equation solver (chip #2) [30] ICs were fully tested and verified the functionality.

Conclusion

- Analog Computing is suitable for specialized computing tasks such as in scientific computing where high speed and high energy efficiency is required, but with less programability.
- Analog computers can be incorporated with digital platforms to improve the performance, leading to hybrid computing.
- Two analog computing methods have been introduced to compute the continuous-time solution of PDEs.
- The proposed methods were verified using the electromagnetic wave equation .
- An AC for solving wave equation has been designed, laid out, and fabricated using 180 nm CMOS technology.
- Speed-up results are provided compared to GPU-, CPU- and FPGA-based FDTD solvers.
- The demonstrated continuous-time wave equation solver IC shows a 420$\times$ speed-up improvement compared to NVIDIA GeForce GTX 1080 Ti GPU while consuming 1000$\times$ less power at the cost of difficulty in programming and low precision.

Publications I

- **A Radio Frequency Analog Computer for Computational Electromagnetics,** N. Udayanga, A. Madanayake, S. I. Hariharan, J. Liang, S. Mandal, L. Belostotski, and L. T. Bruton, IEEE Journal of Solid-State Circuits, vol. 56, no. 2, pp. 440-454, Feb 2021.
- **An Offset-Cancelling Discrete-Time Analog Computer for Solving 1-D Wave Equations,** J. Liang, N. Udayanga, A. Madanayake, S. I. Hariharan and S. Mandal, IEEE Journal of Solid-State Circuits, vol. 56, no. 9, pp. 2881-2894, Sept. 2021.
- **Continuous-Time Algorithms for Solving Maxwell's Equations Using Analog Circuits,** N. Udayanga, S. I. Hariharan, S. Mandal, L. Belostotski, L. T. Bruton and A. Madanayake, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 10, pp. 3941-3954, Oct. 2019.
- **A Fast and Fully-Parallel Analog CMOS Solver for Nonlinear PDEs,** H. Malavipathirana, S.I. Hariharan, N. Udayanga, S. Mandal, and A. Madanayake, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 8, pp. 3363-3376, Aug 2021.

Publications II

- **A Switched-Capacitor-Based Analog Computer for Solving the 1-D Wave Equation**, J. Liang, N. Udayanga, A. Madanayake, S. I. Hariharan and S. Mandal, in IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1-5.
- **Continuous-time Analog Computing Circuits for Solving The Electromagnetic Wave Equation,** N. Udayanga, A. Madanayake, and S. I. Hariharan, in IEEE International Symposium on Circuits and Systems (ISCAS), May 2018, pp. 1-5.
- **Continuous-time algorithms for solving the electromagnetic wave equation in analog ICs,** N. Udayanga and A. Madanayake and S. I. Hariharan, in IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), Aug 2017, pp. 29-32.

Acknowledgment

- Financial support from DARPA's Defense Sciences Office (DSO) and Ocius Technologies is gratefully appreciated.
- Special thanks is in order for Dr. Rui Ma, Mitsubishi Electric Research Laboratories.
- Last but not least, a big thank you to Hasantha Malavipathirana for helping out with the slides.

Thank you

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